## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Abdallah Bacha et al.

Group Art Unit:

Serial No.:

Examiner:

15

Filed: March 11, 2004

Attorney Docket No: 068758.0177

Title: Topology for Providing Clock Signals To Multiple Circuit Units on a Circuit

Client Ref.: IO040204PUS/pw

Module

Mail Stop Patent Application Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450

CERTIFICATE OF MAILING VIA EXPRESS MAIL

PURSUANT TO 37 C.F.R. § 1.10, I HEREBY CERTIFY THAT I HAVE INFORMATION AND A REASONABLE BASIS FOR BELIEF THAT THIS CORRESPONDENCE WILL BE DEPOSITED WITH THE U.S. POSTAL SERVICE AS EXPRESS MAIL POST OFFICE TO ADDRESSEE, ON THE DATE BELOW, AND IS ADDRESSED TO:

MAIL STOP PATENT APPLICATION COMMISSIONER FOR PATENTS P.O. Box 1450 ALEXANDRIA, VA 22313-1450

**EXPRESS MAIL LABEL: EV339228843US** DATE OF MAILING:

MARCH 11, 2004

## INFORMATION DISCLOSURE STATEMENT

Sir:

Applicants respectfully request, pursuant to 37 C.F.R. §§1.56, 1.97 and 1.98, that the art listed on the attached PTO-1449 form be considered and cited in the examination of the above-identified application. A copy of the cited art is enclosed for the convenience of the Examiner.

Furthermore, pursuant to 37 C.F.R. §§1.97(g) and (h), no representation is made that these references are material to the patentability of the present application.

As the Information Disclosure Statement is being submitted before the mailing of the first office action on the merits, Applicants believe that no fee is required. If a fee is

required, please accept this transmittal as a petition therefor and charge any fee to Baker Botts L.L.P. (formerly, Baker & Botts, L.L.P.) Deposit Account No. 02-0383, Order No. (068758.0177) for any other charges necessary for the filing of this Information Disclosure Statement.

BAKER BOTTS L.L.P. (023640)

Date: March 11, 2004

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PTO	-1449			Application No.		Applicant(s): Abdallah Bacha et al.			
			Information Disclosure Citation in an Application		Group A	Group Art Unit		Filing Date	
				068758.0177	068758.0177		March 11, 2004		
				U.S. PATENT DOCUMENTS	,				
		DOCUMENT NO.	DATE	NAME	CLASS	CLASS SUBCLASS		S FILING DATE	
	1	2001/0050856 A1	12-13-01	Matsuzaki	365	365 1		06-06-01	
	2	6,081,145	06-27-00	Bandai et al.	327	327 231		06-11-98	
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				FOREIGN PATENT DOCUMEN	NTS				
		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUBCLAS	S TRANSI	ATION NO	
	3	07-084665	03-31-95	Japan	G06F	1/04	х		
				NON-PATENT DOCUMENTS	S				
		DOCUMENT (Including Author, Title, Source, and Pertinent Pages)					DA	DATE	
	4	"Nested Phase-Lock Loops for Board Level Clocking"; IBM Technical Disclosure Bulletin, Vol. 37, No. 06A; pp. 349-51					ol. June	June 1994	
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EXAMINER					DATE CONSID	ERED			
EXA	MINER	: Initial if citation consider Include copy of this form w	ed, whether or not c ith next communica	tation is in conformance with MPEP ion to the applicant.	§ 609. Draw line thr	ough citation if	not in conformanc	e and not	